

TM5184ALT H.264/AVC 1080 60p Codec LSI

Powered by original computing algorithm “DMNA” based on mathematical methods

1 Features

- Encode and decode up to 1920x1080 size with 60 fps
- 6-channel encoder and decoder function
- Low bit rate (2 Mbps @ full HD -), high image quality, low latency, low power consumption
- Built-in memory controller for DDR2-533, selectable bus width from 16/32/64 bits
- I-Picture Only Mode that needs no external memory devices
- JPEG and H.264/AVC encoders work at the same time

2 Specifications Overview

<H.264/AVC Encoder / Decoder>

- Stream Standard: ISO/IEC 14496 - 10/ITU-T Rec. H.264
- Profile: Baseline Profile Level 1.1 - 4.2 (Encoder) / 1.0 - 4.2 (Decoder)
- Input Video Format: Macro block format (YCbCr420)
- Video Size: Progressive 320x240 - 1920x1080 (Encoder) / 80x96 - 1920x1080 (Decoder)
- Frame Rate: up to 60 fps
- Bit Rate Control: VBR, CBR
- Multi-channel: 1 to 16 channels
- Low Latency: under 100 mSec

<JPEG Encoder>

- Stream standard: ISO/IEC 10918-1 Baseline Encoder
- Input Video Format: Macro block format (YCbCr420)

<Interface>

- Host Interface: Synchronous standard memory bus (Address:16bits, Data: 6bits)
- Video Port: Req-Ack 32 bits
- Bit Stream Port: Req-Ack 32 bits
- SDRAM Interface: Built-In DDR2-533 Memory Controller, Selectable 16/32/64 bits bus width
- JPEG Interface: 8/16 bits data width

<Clock Input>

- 66.66MHz (DDR2)
- 27MHz (Internal Logic)
- Up to 40MHz (Host Interface)

Contact Information

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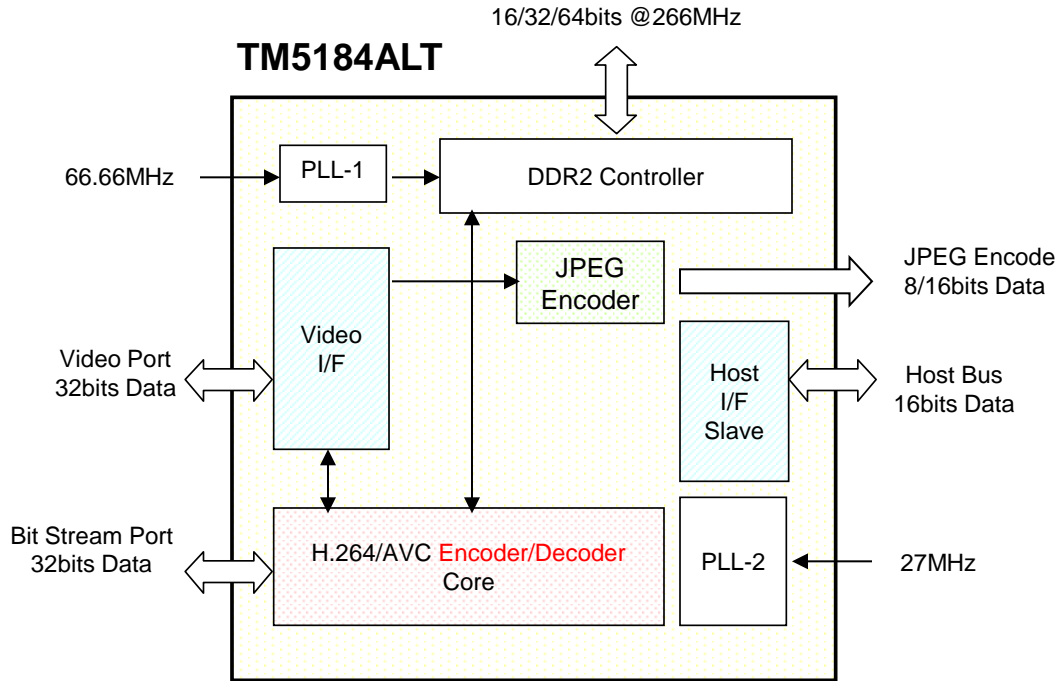
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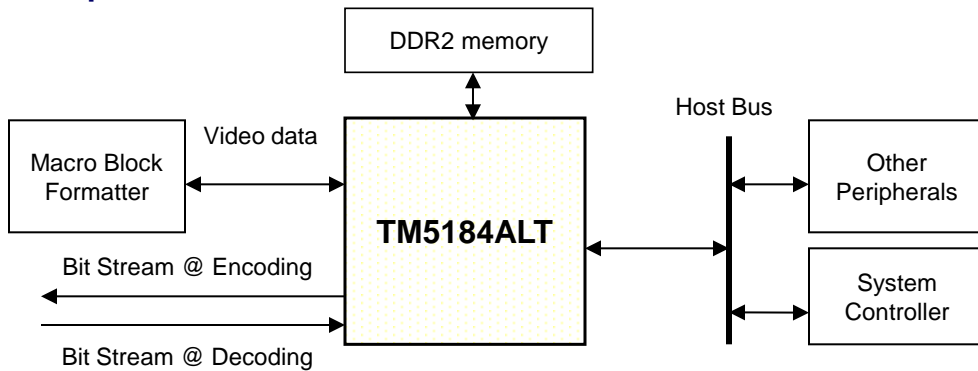
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3 Block Diagram



4 System Example



5 Packaged Materials

- Documents
 - . Datasheet (Hardware Specifications, Software Flow Specifications)
 - . Design Guideline
 - . System Guideline
- Reference Data
 - . Board Schematics
 - . Garber Data
 - . IBIS Data

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