

MPEG-2 Main Profile Encoder/Decoder

Powered by original computing algorithm “DMNA” based on mathematical methods

1 Abstract

- TMC’s MPEG-2 core (RTL-IP) is designed to be compliant with the MPEG-2 Video, which is a highly efficient image compression method standardized by ISO/EC 13818-2. TMC’s RTL is fully verified to function in FPGA.
- Suitable for various applications, such as image processing for high definition television, digital video cameras, and streaming systems through HD network.

2 Specifications

- Compliant with MPEG-2 Video MP@ML, MP@HL-1440, MP@HL
- Bit rate : up to 45Mbps
- Frame rate : up to 60fps
- Video formats : YCbCr 4:2:0
(1080i/60, 1080i/60(1440), 720p/60, 1080p/30, 576p/60, 480p/60)
- Optional functions : error concealment, filter enhancing image quality

3 Features

- Maximum image size : interlace 1080i(1920 x 1080)30fps
: progressive 720p(1280 x 720)60fps
- Encode/Decode functions
- Low power consumption
- 1/2 pixel motion compensation
- Flexible interface for a wide range of processors
- Verified to function in FPGA
- New algorithm, DMNA, is implemented for MPEG-2 Video
- High quality picture encoding



4 Performance

Operation	Image size	fps
MPEG-2 Encode/Decode	1080i(1920×1080)	30
MPEG-2 Encode/Decode	720p(1280×720)	60
MPEG-2 Encode/Decode	480p(720×480)	60

Note Specifications are subject to change without notice

Contact Information

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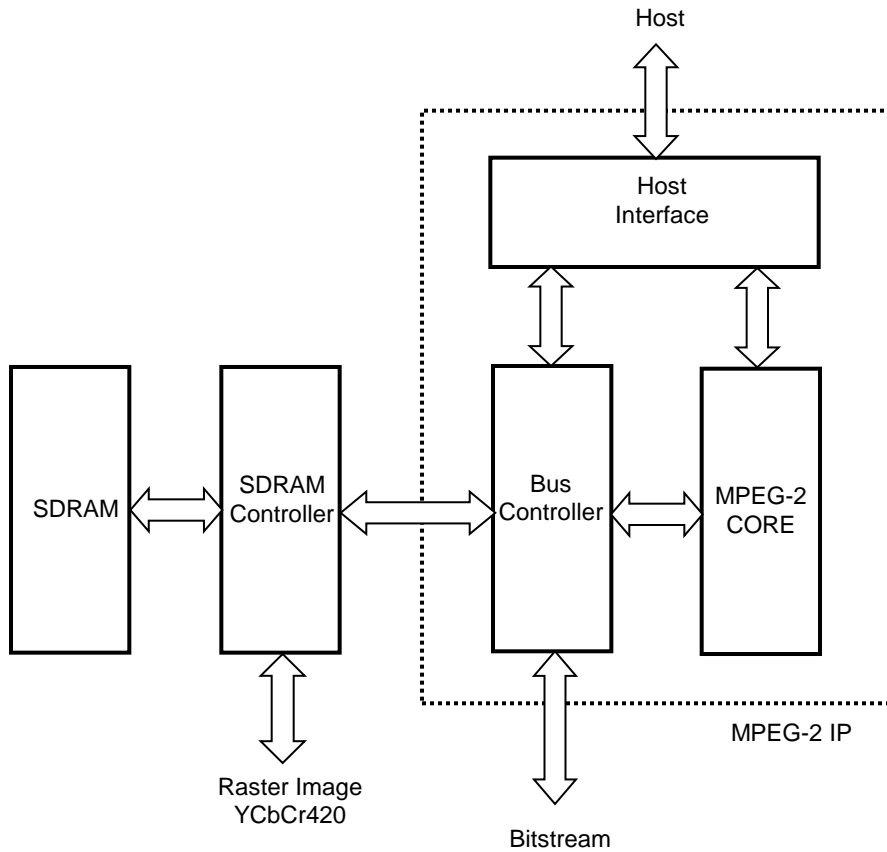
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< MPEG-2 System Block Diagram >

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