JPEG Encoder/Decoder

Powered by original computing algorithm “DMNA” based on mathematical methods

1 Abstract

- Baseline JPEG encoder / decoder described in RTL compliant with ISO/IEC 10918-1
- High speed processing with low clock frequency
- Suitable for digital still camera, printer, facsimile and surveillance camera system

2 Features

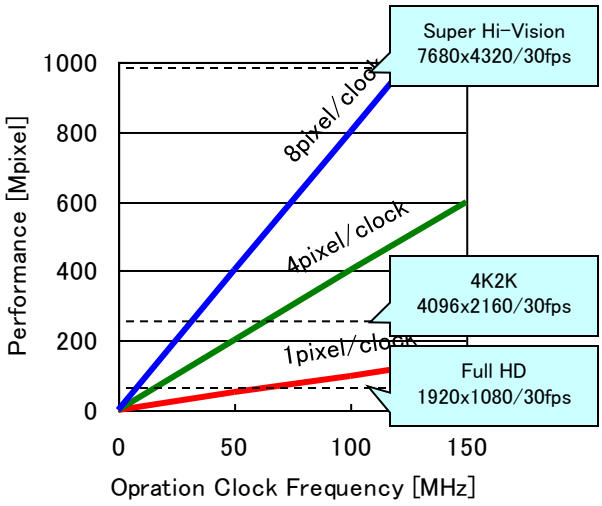
JPEG DMNA

- 3 types of IPs are offered as follows:

performance pixel/clock@4:2:2	Example of performance (4K2K-fps@100MHz)	encoder	decoder	encoder/ decoder
1	12.5 fps	✔	✔	✔
4	50 fps	✔	✔	✔
8	100 fps	✔	–	–

3 Specifications

- Image Format: Frame sequential method.
- Input/Output Format: YCbCr 4:4:4/4:2:2/4:2:0/4:0:0
- Data bus protcol: AXI
- CPU bus protcol: AHB
- Error detection during decoding improper stream
- Tables
  Quantization table (Programmable)
  Huffman table (Programmable)
- Scaling function of Quantization table
- SOI, DHT, DQT, DRI, SOF0, SOS, RSTm, EOI markers



Note Specifications are subject to change without notice

Contact Information
7F, Gotanda NN Bldg., 2-12-19, Nishi-gotanda, Shinagawa-ku, Tokyo 141-0031
Techno Mathematical Co., Ltd.
TEL: +81-3-3492-3633 FAX: +81-3-3492-3631
Email: info-sales@tmath.co.jp URL: https://www.tmath.co.jp/en/